APPENDIX A - CLAIMS

The claims are presented below for convenient reference by the Examiner.

Claims 1-6. (Canceled)

7. (Previously Presented) An integrated circuit including a phase lock loop, the phase lock loop comprising:

a voltage-to-current circuit to influence a voltage on a capacitor;

a voltage controlled oscillator responsive to the voltage on the capacitor to provide a second clock signal; and

a sampling circuit responsive to a first clock signal and the second clock signal, and to generate two voltage values, a difference of the two voltage values being a function of a phase difference between the first and second clock signals.

8. (Original) The integrated circuit of claim 7, wherein the voltage controlled oscillator generates the second clock signal as a differential signal, and wherein the sampling circuit samples the differential signal at transition points of the first clock signal to generate the two voltage values.

9. (Original) The integrated circuit of claim 7, wherein the first clock signal is received as a differential signal, and the sampling circuit samples the differential signal at transition points of the second clock signal to generate the two voltage values.

10. (Original) The integrated circuit of claim 7, wherein the voltage-to-current circuit includes:

a first transconductance amplifier to source a first current when a positive voltage differential exists between the two voltage values;

a second transconductance amplifier to sink a second current when a negative voltage differential exists between the two voltage values; and

an output stage coupled between the first transconductance amplifier and the capacitor, and coupled between the second transconductance amplifier and the capacitor.

11. (Original) The integrated circuit of claim 10, wherein the output stage further includes a complementary pair of transistors.

12. (Original) An integrated circuit, including:

a phase lock loop having a voltage-to-current circuit to influence a voltage on a capacitor; a voltage controlled oscillator responsive to the voltage on the capacitor to provide a second clock signal, and a sampling circuit responsive to a first clock signal and the second clock signal, and to generate two voltage values, a difference of the two voltage values being a function of a phase difference between the first and second clock signals; and

a plurality of sequential elements coupled to the phase lock loop.

13. (Original) The integrated circuit of claim 12, wherein at least one of the plurality of sequential elements is to receive data clocked by a signal provided by the phase lock loop.

14. (Previously Presented) The integrated circuit of claim 12, wherein the plurality of sequential elements includes at least one flip-flop.

15. (Previously Presented) The integrated circuit of claim 12, wherein the voltage-to-current circuit includes a first transconductance amplifier coupled to a first differential input node and a second differential input node, a second transconductance amplifier coupled to the first differential input node and the second differential input node, and a first current mirror, a second current mirror, and a common gate output stage coupled to the first transconductance amplifier and the second transconductance amplifier.

16. (Original) The integrated circuit of claim 15, wherein the voltage-to-current circuit includes a bias circuit to bias a complementary pair of transistors included in the common gate

output stage.

17. (Previously Presented) A phase lock loop, including:

a voltage controlled oscillator to generate a differential signal on two nodes; and

a phase detector to compare a phase of the differential signal and a phase of a received signal, the phase detector including a sampling circuit to periodically sample voltage values on the two nodes, and a linear voltage-to-current converter responsive to the voltage values to create a control voltage for the voltage controlled oscillator.

18. (Previously Presented) The phase lock loop of claim 17 wherein the linear voltage-to-current converter includes:

a first transconductance amplifier to source current when a positive difference exists between the voltage values; and

a second transconductance amplifier to sink current when a negative difference exists between the voltage values.

19. (Previously Presented) The phase lock loop of claim 18, further including an output stage with series connected transistors having gates coupled in common.

20. (Previously Presented) The phase lock loop of claim 17, wherein the sampling circuit is configured to sample the voltage values at a transition point of the received signal.

21. (Previously Presented) The phase lock loop of claim 17 further including:

a frequency divider coupled to the voltage controlled oscillator and to the phase detector.

22. (Previously Presented) The phase lock loop of claim 21, wherein the frequency divider is to provide a differential output signal.

23. (Previously Presented) The integrated circuit of claim 12, wherein the plurality of sequential elements includes a microprocessor.

24. (Previously Presented) The integrated circuit of claim 12, wherein a frequency of the second clock signal comprises approximately an integer multiple of a frequency of the first clock signal.

25. (Previously Presented) The integrated circuit of claim 12, wherein the first clock signal comprises a differential input signal.

26. (Previously Presented) The integrated circuit of claim 12, wherein the sampling circuit is configured to sample a rising edge of the first clock signal.